IN THE CLAIMS

Claims 4 and 6-8 are currently pending, wherein claims 1 – 3 and 5 are canceled without prejudice or disclaimer, and the remaining claims 4 and 6-8 are being amended as follows:

1-3. (Canceled).

4. (Currently Amended) ~~The processor according to Claim 3~~ A processor comprising:

a register file including a plurality of registers assigned with register numbers, each of the registers for storing at least one of operand data and operation result data;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data so as to generate the operation result data;

a first decoder for decoding a first register designating field of an instruction code, said first register designating field having a first register designating number stored therewith, said first decoder further for generating signals designating source register numbers based on the first register designating number so as to be consecutive to each other;

a second decoder for decoding a second register designating field of the instruction code, said second register designating field having a second register designating number stored therewith, said second decoder further for generating signals designating result register numbers based on the second designating register number so as to be consecutive to each other; and

a control circuit for sending the operand data stored in source registers corresponding to the designated source register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data and for sending the operation result data obtained from the at least one operation pipe to result registers corresponding to the designated result register numbers, wherein the plurality of registers are divided into a plurality of banks, and by reading or writing data from the plurality of banks, the number of ports of reading or writing the data of respective banks is restricted to be equal to or smaller than a number of the register designating fields so as to restrain an increase in a circuit scale caused by reading or writing the

data by a number of times larger than the number of the register designating fields contained in the instruction code.

5. (Canceled).

6. (Currently Amended) The processor according to Claim [[3]] 4, wherein a data pack operation, which deals with a number of the data read from the source registers larger than a number of the data written to the result registers, data read from the source registers are larger in a number than a number of the register designating fields contained in the instruction code so as to eliminate invalid portions in the result registers.

7. (Currently Amended) The processor according to Claim [[3]] 4, wherein a data unpack operation, which deals with a number of the data written to the result registers larger than a number of the data read from the source registers, a number of data written in parallel to the result registers is larger than a number of the register designating fields contained in the instruction code so as to avoid data writing a plurality of times.

8. (Currently Amended) The processor according to Claim [[3]] 4, wherein an operation of outputting the data having a data width wider than a width of input data such that a number of data larger than a number of the write register designating fields contained in the instruction code can be written to the results registers so as to eliminate invalid portions in the input data and avoid mounting a special register having a wider data width.